CLAIMS:

1. A method of compiling a software program for a programmable processor having a functional unit associated with at least two issue slots, the method comprising:

receiving a set of processor-executable operations comprising a processor-executable operation of a type typically associated with at least two issue slots; and

replacing the processor-executable operation of the type associated with at least two issue slots of the functional unit with a processor-executable operation associated with fewer than all of the issue slots.

2. The method of claim 1, further comprising analyzing the processor-executable operation of the type typically associated with at least two issue slots and external information to determine whether the processor-executable operation of the type typically associated with at least two issue slots can be replaced by a processor-executable operation associated with fewer than all of the issue slots associated with the functional unit.

3. The method of claim 1, wherein replacing the processor-executable instruction comprises replacing the processor-executable operation of the type typically associated with at least two issue slots with an equivalent processor-executable operation associated with only one issue slot.

4. The method of claim 1, wherein replacing the processor-executable instruction comprises replacing the processor-executable operation of the type typically associated with at least two issue slots with an equivalent processor-executable operation associated with a plurality of issue slots.

5. The method of claim 1, further comprising:

determining a number of input registers and a number of output registers that are used by the processor-executable operation of the type typically associated with at least two issue slots; and

when the processor-executable operation of the type typically associated with at least two issue slots uses at most two input registers and one output register, replacing the

processor-executable operation of the type typically associated with at least two issue slots with an equivalent processor-executable operation associated with only one issue slot.

6. The method of claim 1, further comprising:

identifying any source operations of the set of processor-executable operations that produce a result affecting a result of a selected processor-executable operation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed;

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the selected processor-executable operation; and

when the selected processor-executable operation can be replaced by a processor-executable operation associated with fewer than all of the issue slots associated with the functional unit, substituting an equivalent processor-executable operation associated with fewer than all of the issue slots associated with the functional unit.

7. The method of claim 6, further comprising:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the selected processor-executable operation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the selected processor-executable operation can be constructed using the subsequent instruction word.

8. The method of claim 1, wherein the processor-executable operation of the type typically associated with at least two issue slots is a shuffle operation.

9. The method of claim 1, wherein the processor-executable operation of the type typically associated with at least two issue slots is a floating point operation.

10. A method of compiling a software program for a programmable processor having a functional unit associated with a plurality of issue slots, the method comprising:

receiving a processor-executable superoperation of a type typically associated with at least two issue slots;

determining a number of input registers and a number of output registers that are used by the superoperation; and

when the superoperation uses at most two input registers and one output register, replacing the superoperation with an equivalent processor-executable operation associated with only one issue slot.

11. The method of claim 10, further comprising:

identifying any source operations that produce a result affecting a result of the superoperation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed; and

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the superoperation.

12. The method of claim 11, further comprising:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation can be constructed using the subsequent instruction word.

13. The method of claim 10, wherein the superoperation is a shuffle operation.

14. The method of claim 10, wherein the superoperation is a floating point operation.

15. A method of executing an instruction by a processor having a functional unit associated with a plurality of issue slots, the method comprising:

determining whether the instruction can be executed using fewer than all of the issue slots associated with the functional unit;

when the instruction can be executed using fewer than all of the issue slots associated with the functional unit, mapping the instruction to fewer than all of the issue slots.

16. The method of claim 15, further comprising analyzing the instruction and external information to determine whether the instruction can be executed using fewer than all of the issue slots associated with the functional unit.

17. The method of claim 15, further comprising:

determining a number of input registers and a number of output registers that are used by the instruction; and

when the instruction uses at most two input registers and one output register, mapping the instruction to a single issue slot.

18. The method of claim 15, further comprising mapping the instruction to a single issue slot.

19. The method of claim 18, further comprising determining which one of the plurality of issue slots to map to the instruction.

20. The method of claim 15, further comprising mapping the instruction to a plurality of issue slots.

21. The method of claim 15, wherein the instruction is a shuffle operation.

22. The method of claim 15, wherein the instruction is a floating point operation.

23. A processor-readable medium containing processor-executable instructions for:

receiving a set of operations comprising a operation of a type typically associated with at least two issue slots of a functional unit of a programmable processor; and

replacing the operation of the type typically associated with at least two issue slots by a operation associated with fewer than all of the issue slots associated with the functional unit.

24. The processor-readable medium of claim 23, further containing processor-executable instructions for analyzing the operation of the type typically associated with at least two issue slots and external information to determine whether the operation of the type typically associated with at least two issue slots can be replaced by a operation associated with fewer than all of the issue slots associated with the functional unit.

25. The processor-readable medium of claim 23, further containing processor-executable instructions for replacing the operation of the type typically associated with at least two issue slots with an equivalent operation associated with only one issue slot.

26. The processor-readable medium of claim 23, further containing processor-executable instructions for:

determining a number of input registers and a number of output registers that are used by the operation of the type typically associated with at least two issue slots; and

when the operation of the type typically associated with at least two issue slots uses at most two input registers and one output register, replacing the operation of the type typically associated with at least two issue slots with an equivalent operation associated with only one issue slot.

27. The processor-readable medium of claim 23, further containing processor-executable instructions for:

identifying any source operations of the set of operations that produce a result affecting a result of a selected operation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed;

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the selected operation; and

when the selected operation can be replaced by a operation associated with fewer than all of the issue slots associated with the functional unit, substituting an equivalent operation associated with fewer than all of the issue slots associated with the functional unit.

28. The processor-readable medium of claim 27, further containing processor-executable instructions for:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the selected operation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the selected operation can be constructed using the subsequent instruction word.

29. The processor-readable medium of claim 23, wherein the operation of the type typically associated with at least two issue slots is a shuffle operation.

30. The processor-readable medium of claim 23, wherein the operation of the type typically associated with at least two issue slots is a floating point operation.

31. A processor-readable medium containing processor-executable instructions for:

receiving a superoperation of a type typically associated with at least two issue slots of a functional unit of a programmable processor;

determining a number of input registers and a number of output registers that are used by the superoperation; and

when the superoperation uses at most two input registers and one output register, replacing the superoperation with an equivalent operation associated with only one issue slot.

32. The processor-readable medium of claim 31, further containing processor-executable instructions for:

identifying any source operations that produce a result affecting a result of the superoperation;

placing commands for the source operations in instruction words;

selecting an earliest instruction word from a set of instruction words after the instruction words in which commands for the source operations have already been placed; and

determining whether an instruction word can be constructed that contains any commands already included in the earliest instruction word in addition to a command for the superoperation.

33. The processor-readable medium of claim 32, further containing processor-executable instructions for:

when an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation cannot be constructed, selecting a subsequent instruction word; and

determining whether an instruction word that contains any commands already included in the earliest instruction word in addition to the command for the superoperation can be constructed using the subsequent instruction word.

34. The processor-readable medium of claim 31, wherein the superoperation is a shuffle operation.

35. The processor-readable medium of claim 31, wherein the superoperation is a floating point operation.

36. A processor-readable medium containing processor-executable instructions for:

determining whether the instruction can be executed using fewer than all issue slots associated with a functional unit of a processor;

when the instruction can be executed using fewer than all issue slots associated with the functional unit, mapping the instruction to fewer than all issue slots.

37. The processor-readable medium of claim 36, further containing processor-executable instructions for analyzing the instruction and external information to determine whether the instruction can be executed using fewer than all issue slots associated with the functional unit.

38. The processor-readable medium of claim 36, further containing processor-executable instructions for:

determining a number of input registers and a number of output registers that are used by the instruction; and

when the instruction uses at most two input registers and one output register, mapping the instruction to a single issue slot.

39. The processor-readable medium of claim 36, further containing processor-executable instructions for mapping the instruction to a single issue slot.

40. The processor-readable medium of claim 39, further containing processor-executable instructions for determining which one of the plurality of issue slots to map to the instruction.

41. The processor-readable medium of claim 36, further containing processor-executable instructions for mapping the instruction to a plurality of issue slots.

42. The processor-readable medium of claim 36, wherein the instruction is a shuffle operation.

43. The processor-readable medium of claim 36, wherein the instruction is a floating point operation.